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10/055,992	01/28/2002	Norifumi Kobayashi	02887.0213	2127

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FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER LLP
901 NEW YORK AVENUE, NW
WASHINGTON, DC 20001-4413

EXAMINER	
PROCTOR, JASON SCOTT	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 07/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/055,992	KOBAYASHI ET AL.	
	Examiner	Art Unit	
	Jason Proctor	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 April 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/28/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-21 have been presented for examination. Claims 1-21 have been rejected.

Specification

1. The disclosure is objected to because of the following informalities: page 13, line 26 contains a typographical error "Logi0cal". Page 19, lines 21-26 appears to contain at least one typographical error in "[...] the series of procedures described in these embodiments are never procedures capable of being executed only a dedicated purpose machine."

Appropriate correction is required.

Claim Objections

2. Claim 5 is objected to because of the following informalities: lines 4-5 of the claim contains the typographical error "verification whether abnormality is caused". The Examiner presumes this should read "verifying whether abnormality is caused" as in claims 12 and 19.

Claim 15 is objected to because of the following informalities: line 6 of the claim contains the typographical error "8comprising". Appropriate correction is required.

Applicants' use of the term "dispersion", especially in "dispersion of signal level" and "dispersion in power supply voltage" as in claim 6, appears to be unconventional. While Applicants may be their own lexicographer, the precise meaning of this term as used by Applicants is unclear. The Examiner respectfully requests that Applicants' response include

citation of the portion of the specification that particularly defines the claim terminology using the term "dispersion" or provide references that particularly define the term as known in the art.

Claim Rejections - 35 USC § 101

35 U.S.C. § 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 8-14 rejected under 35 U.S.C. § 101 because the claimed invention is directed to non-statutory subject matter. Claims 8-14 recite a method that, given its broadest reasonable interpretation, is not limited to the technological arts. For example, the method of claim 8 could be performed by a human being with pencil and paper. The step of "executing a logical simulation of the integrated circuit" is a common classroom exercise for students of computer science. The method is nonstatutory as it defines a mental process. The Examiner respectfully suggests claiming a "computer-executed method" or some equivalent.

To expedite a complete examination of the instant application the claims rejected under 35 U.S.C. § 101 (nonstatutory) above are further rejected as set forth below in anticipation of applicant amending these claims to place them within the four statutory categories of invention.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. § 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 2, 6, 9, 16, and 20 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

5. Claims 2, 9, and 16 recite limitations wherein the "[the method or a component] corrects said design information on the basis of said dispersion" as in representative claim 2. The disclosure does not describe this step of correcting the design information. The "correction" described by the specification (for example, page 9, lines 10-18; page 16, lines 11-29) concerns forming a *more accurate* delay model (see especially page 16, lines 24-29) and does not, as these claims recite, "correct said design information on the basis of said dispersion". Here, "design information" is interpreted as the *circuit layout design data* (or an equivalent term) necessary to define the groups required by the method (for example, Fig. 3 and related descriptions in the specification) and distinct from the *dispersion rule file*. Given their broadest reasonable interpretation, these claims recite that the method manipulates the *circuit layout design data* to "correct" a dispersion, such as repositioning circuit elements to overcome a malfunction in the circuit design. This step is not described by the specification.

The following is a quotation of the second paragraph of 35 U.S.C. § 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 5, 12, and 19 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

These claims are rejected for several reasons.

These claims recite the limitation "said signal" which has insufficient antecedent basis in all three claims.

These claims recite the limitation "said power supply voltage" which has insufficient antecedent basis in all three claims.

The claim recites "verifying whether abnormality is caused in the transmission of said signal by the difference in said power supply voltage in the same chip" which has at least two distinct interpretations. A first interpretation could be summarized as "Determining, by examining a difference in power supply voltage, whether abnormality has occurred." The output from this first interpretation indicates the presence or absence of abnormality. A second interpretation could be summarized as "Given that abnormality has occurred, determine whether it was caused by a difference in power supply voltage." The output from this second interpretation indicates whether the power supply voltage is the cause of the abnormality. As a result, it is impossible to determine the metes and bounds defined by this limitation.

Aside from the lack of antecedent basis for "said power supply voltage", it is unclear whether "the difference in said power supply voltage in the same chip" refers to a situation wherein different power supply voltages are tested on the same chip, a situation wherein the power supply voltage is conditioned differently (creating a "difference in said power supply voltage"), or a situation wherein different portions of the chip receive different power supply

voltages. Primarily, it is unclear how to interpret "differences" in said power supply voltage (indicating a single power supply voltage.) The claim language requires significant implied details in order to have a definite meaning.

7. Claims 8-14 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 8 recites the limitation "said design information" in line 8 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claims rejected but not specifically mentioned stand rejected by virtue of their dependence.

Claim Interpretation

In the interest of compact prosecution, the Examiner makes the following claim interpretations in order to apply prior art to the claims. See *Ex parte Ionescu*, 222 USPQ 537 (Bd. Pat. App. & Inter. 1984).

Claims 2, 9, and 16 are interpreted according the teachings of the specification, particularly page 16, lines 11-29, wherein "correction" refers to an improved delay calculation.

Claim 8 is interpreted as the method performed by the system of claim 1.

Claims 5, 12, and 19 are interpreted as "the logical simulation system considers power supply voltage in the delay calculation."

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1-21 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,484,297 to Dixit et al. (Dixit).

Regarding claim 1, Dixit discloses a logical simulation system [*"The present invention generates the delay data points (Dnom) by conducting SPICE simulation on the cell* [...]" (column 5, lines 7-20)] comprising:

A component that receives information regarding the electrical and physical characteristics which influence the operation of an integrated circuit, the functional equivalence of a "dispersion rule file" ["[...] *conducting a SPICE simulation on the cell by using the parameters for the nominal condition (i.e., nominal P* [process], *V* [voltage], *and T* [temperature]*) and the transistor level netlist of the cell. However, during the simulation, the input ramptime (R) and the output load (F) of the cell are varied within a respective range."* (column 5, lines 7-20) Dixit implicitly discloses the SPICE simulation component that receives both the nominal P, V, and T data as well as the varied R and F data.];

A component which receives design information ["[...] *conducting a SPICE simulation on the cell by using the parameters for the nominal condition (i.e., nominal P* [process], *V*

[voltage], *and T* [temperature]*) and the transistor level netlist of the cell.* (column 5, lines 7-20) Dixit implicitly discloses the SPICE simulation component that receives the "design information".];

Prepares delay information in consideration of each influence of said information regarding the electrical and physical characteristics which influence the operation of an integrated circuit on the basis of that information and the design information [*"*[...] *delays are computed by considering not only the process (P), voltage (V), temperature (T) but also input ramptime (R) and output load or fanout (F) of the cells.* (column 4, line 66 – column 5, line 6); *"In step 140, after solving for Kp, Kt, and Kv, they are applied to the following equation to solve for any new delays for the cells* [...]" (column 7, lines 45-59)]; and

And a logical simulation part which receives said design information and said delay information to carry out a logical simulation of the integrated circuit [*"The present invention provides for accurate calculation of delays for cells in ASICs."* (column 4, lines 32-45); The utility of a delay calculation in an integrated circuit cell is to accurately simulate the integrated circuit. Dixit discloses the use of a SPICE simulator that uses a delay calculation (column 5, lines 7-20). Dixit therefore implicitly discloses an improved delay calculation for use in a SPICE simulator.]

Claim 8 recites the method performed by the system of claim 1. Dixit teaches a computer-implemented method (column 7, line 60 – column 8, line 10) and is therefore rejected for the same reasons given above for claim 1.

Claim 15 recites a computer-readable recorded medium which causes a computer to execute the method of claim 1. Dixit teaches a computer-implemented method (column 7, line 60 – column 8, line 10) and is therefore rejected for the same reasons given above for claim 1.

Regarding claims 2, 9, and 16, Dixit discloses finding an improved delay calculation to be used in a SPICE circuit simulation [*"[...] propagation delays and the setup/hold time delays are computed by considering not only the process (P), voltage (V), temperature (T) but also input ramptime (R) and output load or fanout (F) of the cells* [...]" (column 4, lines 33-46)].

Regarding claims 3, 10, and 17, Dixit discloses classifying said information on dispersion into groups of an optional size which constitute the chip [*"The integrated circuit 26 further comprises a large number* [...] *of small cells 32. Each cell 32 represents a single logic element, such as a gate, or several logic elements interconnected in a standardized manner to perform a specific function."* (column 2, lines 28-35) *"It is an object of the present invention to provide methods for calculating delays for cells in an ASIC."* (column 4, lines 29-31)].

Regarding claims 4, 11, and 18, Dixit discloses that the design information includes actual configuration information which is information on the position of a cell of the integrated circuit in an actual configuration [*"The output of partitioning is a set of blocks, along with the interconnections required between blocks. The set of interconnections required is the netlist."* (column 2, lines 59-67); *"The present invention generates the delay data points (Dnom) by conducting SPICE simulation on the cell by using the parameters for the nominal condition* [...]

and the transistor level netlist of the cell." (column 5, lines 7-20) As used by Dixit, "netlist" meets the broadest reasonable interpretation of "information on the position of a cell of the integrated circuit in an actual configuration".]

Regarding claims 5, 12, and 19, Dixit discloses that the method considers power supply voltage in the delay calculation [*"A new delay can be solved for any given new P, V, T, R and F by using the above equation."* (column 7, lines 45-59)].

Regarding claims 6, 13, and 20, Dixit discloses that the electrical and physical characteristics include a power supply voltage [*"[...] delays are computed by considering not only the [...] voltage"* (column 4, lines 33-46)] and the method calculates the effects of dispersion in the power supply voltage and a delay time [*"A new delay can be solved for any given new P, V, T, R and F using the above equation."* (column 7, lines 45-59)].

Regarding claims 7, 14, and 21, Dixit discloses that design information includes information on wiring [*"Each of the cells of an IC may have one or more pins, each of which, in turn, may be connected to one or more other pins of the IC by wires."* (column 1, lines 18-25); *"Although not visible in the drawing, the various elements of the circuit 26 are interconnected by electrically conductive lines or traces [...]"* (column 2, lines 36-44)].

The logical simulation method comprises dividing said information on wiring into segments corresponding to the size of the group and the delay information is prepared so that the influence of said dispersion is considered for every segment [*"The output of partitioning is a set*

of blocks, along with the interconnections required between blocks. The set of interconnections required is the netlist." (column 2, lines 59-67); *"The present invention generates the delay data points (Dnom) by conducting SPICE simulation on the cell by using the parameters for the nominal condition* [...] *and the transistor level netlist of the cell."* (column 5, lines 7-20)].

Conclusion

Art considered pertinent by the examiner but not applied has been cited on form PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached at (571) 272-3749. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov.

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Jason Proctor
Examiner
Art Unit 2123

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Paul L. Rodriguez 7/22/05
Primary Examiner
Art Unit 2125